HGA045NE4SL

9 1 &K 3RZHU (

V_{DS}		45	V
$R_{DS(on),typ}$	V_{GS}=10V	3.5	m :
$R_{DS(on),typ}$	V_{GS}=4.5V	4.6	m :
$I_{D\ (Sillicon\ Limited)}$		59	A

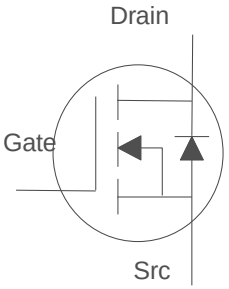
Feature

- Optimized for high speed switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

TO-220F



Part Number	Package	Marking
HGA045NE4SL	TO-220F	GA045NE4SL

1 2 3

Absolute Maximum Ratings at T_j X Q O H V V R W K H U Z L V H V S H F L I L H G

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C	59	A
		T_C	42	
Drain to Source Voltage	V_{DS}	-	45	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	200	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C	60	mJ
3 R Z H U ' L V V L S D W L R Q	P_D	T_C	33	:
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	4.5	:
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	60	:

[redacted]

		V_{GS}=0V, V_{DS} 9 I 0 +]	-			pF
	C_{rss}		-			
Total Gate Charge (10V)	Q_g (10V)		-	42	-	
Total Gate Charge (4.5V)	Q_g (4.5V)	V_{DD}=20V, I_D=20A, V_{GS}=10V	-	22	-	nC
Gate to Source Charge	Q_{gs}		-	4	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn on Delay Time	$t_{d(on)}$		-	12	-	
Rise time	t_r	V_{DD}=20V, I_D=20A, V_{GS}=10V,	-	10	-	ns
7 X U Q R I I ' H O D \ 7 L P H	$t_{G\ RII}$	R_G=10 : ,	-	41	-	
Fall Time	t_I		-	16	-	

Reverse Diode Characteristics

		V_{GS}=0V, I_F=20A	-	0.9	1.2	
			-	30	-	nC

Fig 1. Typical Output Characteristics

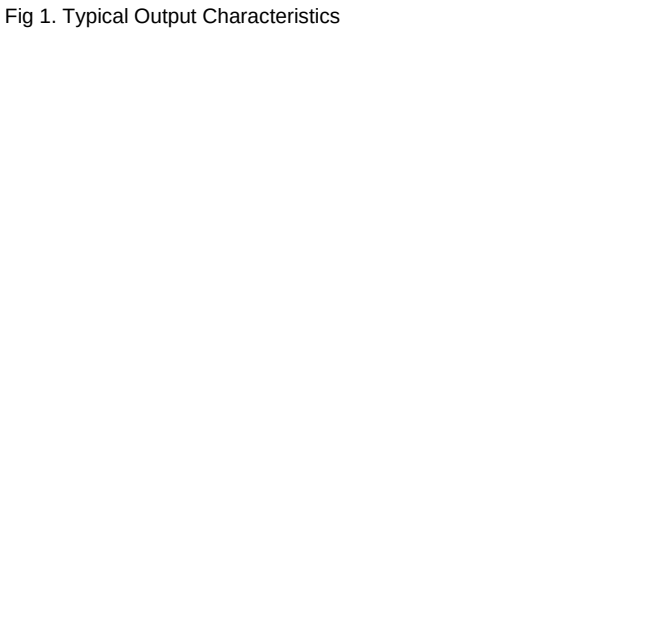
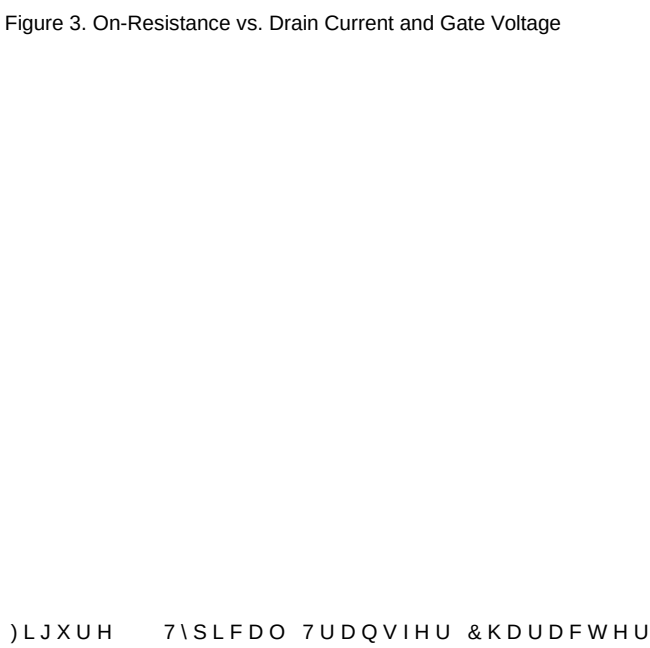
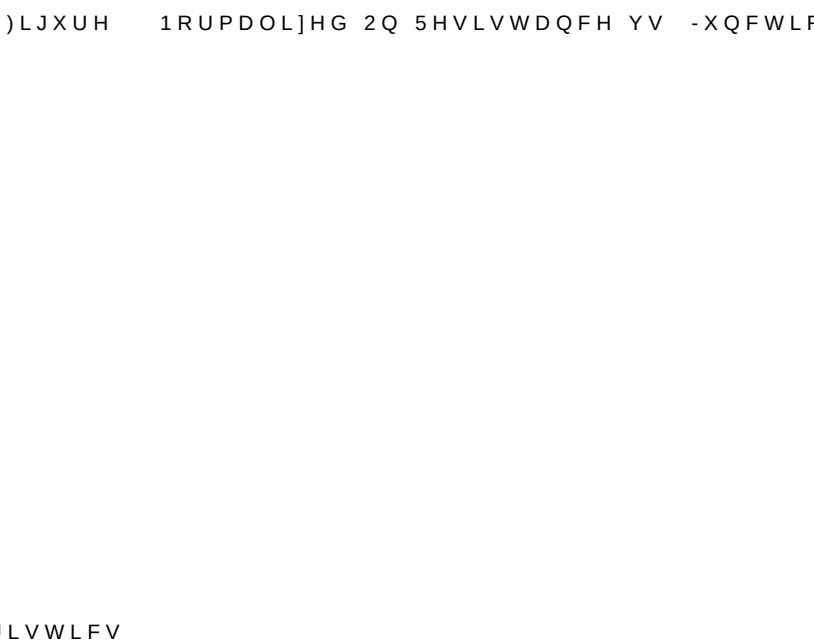


Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage



)LJXUH 1RUPDOL]HG 2Q 5HVLVWDQFH YV -XQFWLRQ



)LJXUH 7\SLFDO 7UDQVIHU &KDUDFWHULVWLFV

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

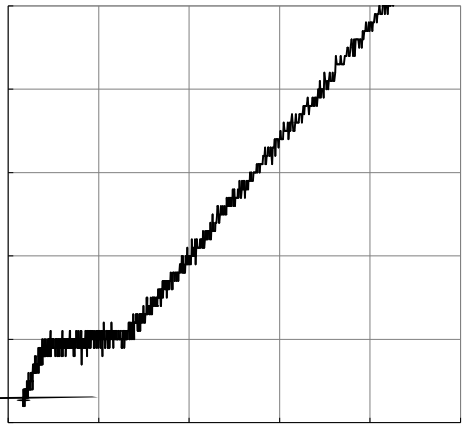


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

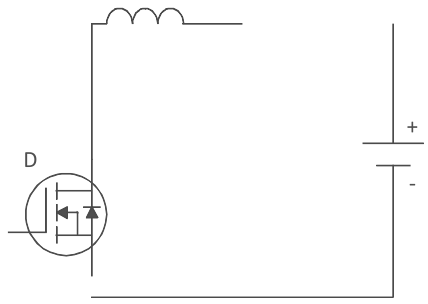
)LJXUH 0D[LPXP 6DIH 2SHUDWLQJ $UHD

Figure 10. Maximun Drain Current vs. Case Temperature

)LJXUH 1RUPDOL]HG 0D[LPXP 7UDQVLHQW 7KHUPDO ,PSHGDQFH -XQFWLR

,QGXFWLYH VZLWFKLQJ 7HVW	

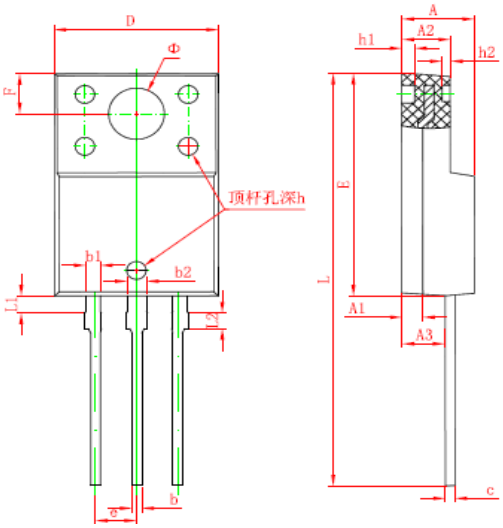
Gate Charge Test	

8FODPSHG ,QGXFWLYH 6ZLWFKLQJ 8,6 7HVW	
	

Diode Recovery Test	

Package Outline

TO-220F, 3 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.350	4.650	0.169	0.185
A1	1.300 REF.		0.051 REF.	
A2	2.850	3.150	0.112	0.124
A3	2.500	2.900	0.102	0.119
b	0.700	0.900	0.028	0.035
b1	0.700	1.000	0.028	0.039
b2	1.270	1.570	0.050	0.062
c	0.430	0.740	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540 TYP.		0.100 TYP.	
F	2.700 REF.		0.106 REF.	
Φ	3.500 REF.		0.138 REF.	
h	0.000	0.300	0.000	0.012
h1	0.800 REF.		0.031 REF.	
h2	0.500 REF.		0.020 REF.	
L	28.000	28.400	1.102	1.118
L1	1.100	1.300	0.043	0.051
L2	0.920	1.040	0.036	0.043